

MATLAB EXPO 2019

Wired Communications Systems Modeling and Analysis

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Development Manager, MathWorks

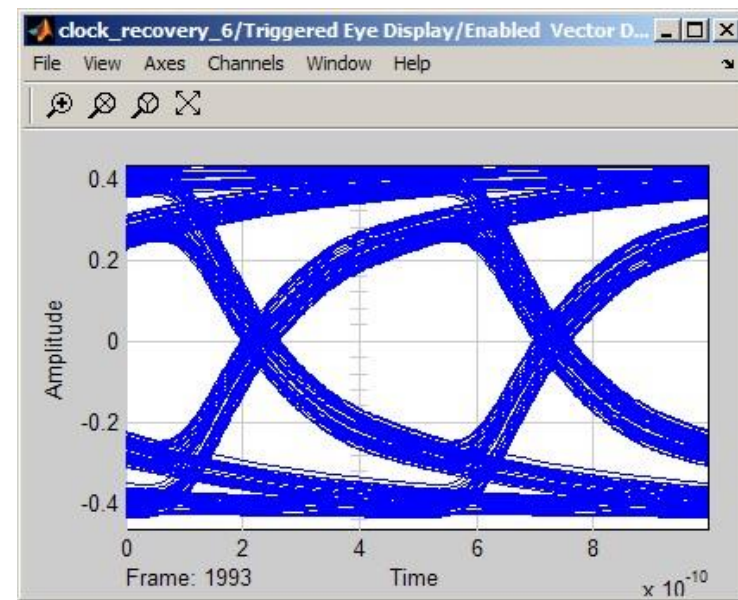
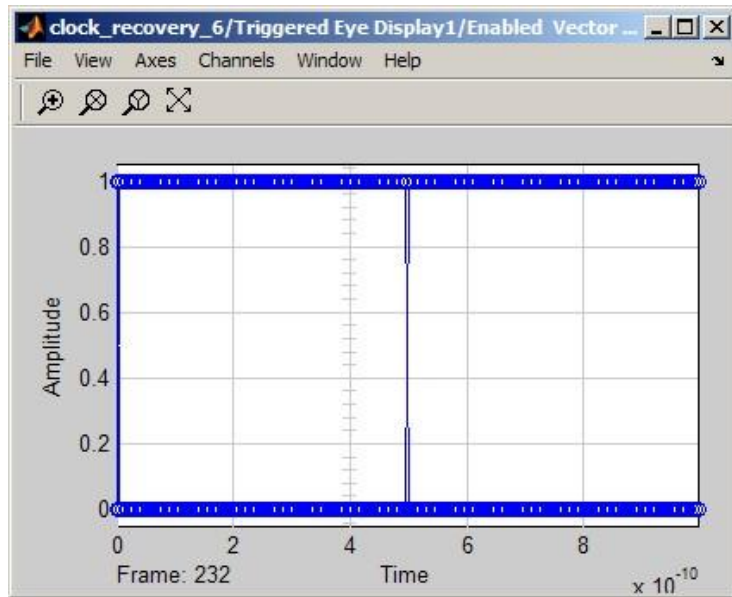


What's Covered

- Introduction to SerDes Design and Signal Integrity Analysis
- Using SerDes Toolbox for System-Level Design and Analysis
- Automatic Generation of Standard Compliant IBIS-AMI Models
- SerDes Verification Using Channel Simulators

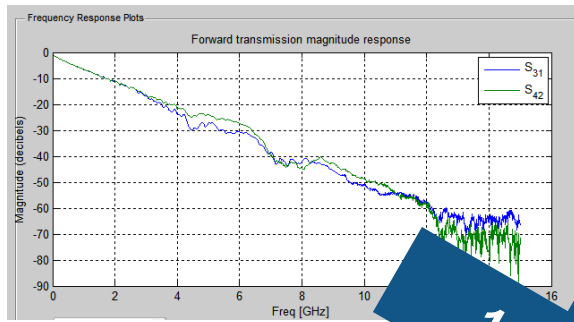
Introduction to SerDes Design and Signal Integrity Analysis

What is Signal Integrity?

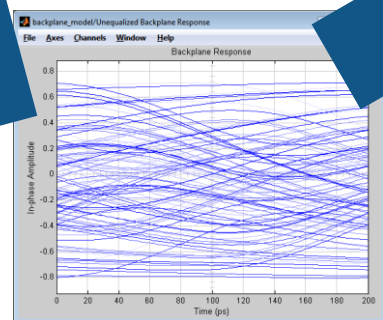


Typical SerDes Design Workflow

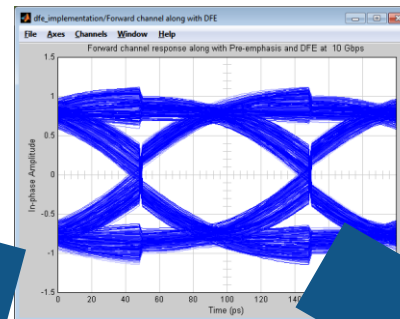
1. Time-domain characterization of the channel
2. Design of analog and digital equalizers
3. Simulation of the system performance in the time domain
4. Hardware implementation and IP verification
5. IBIS-AMI model generation and SerDes system verification



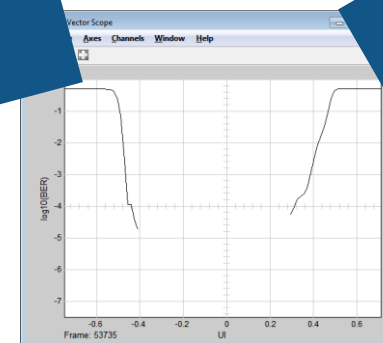
1



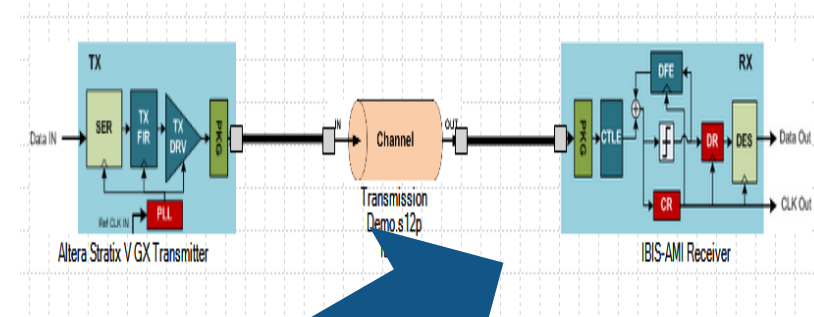
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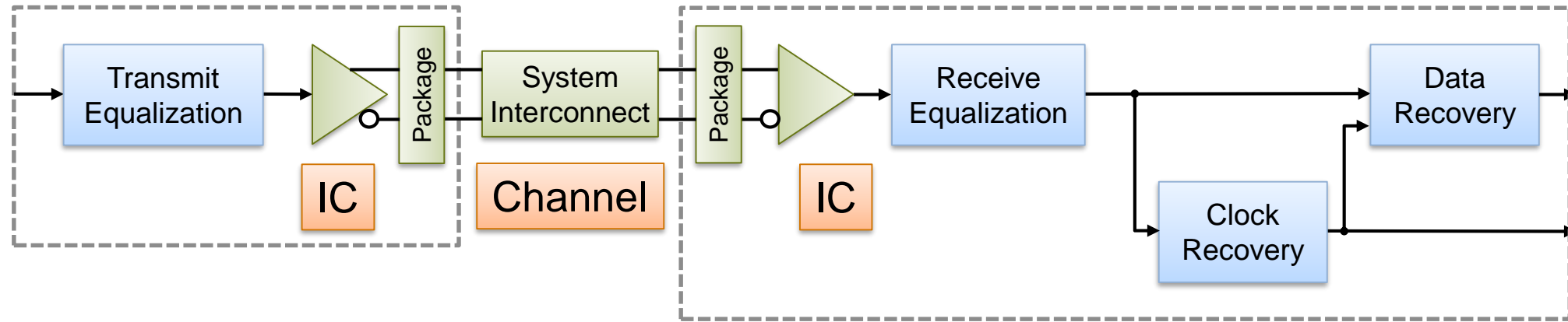
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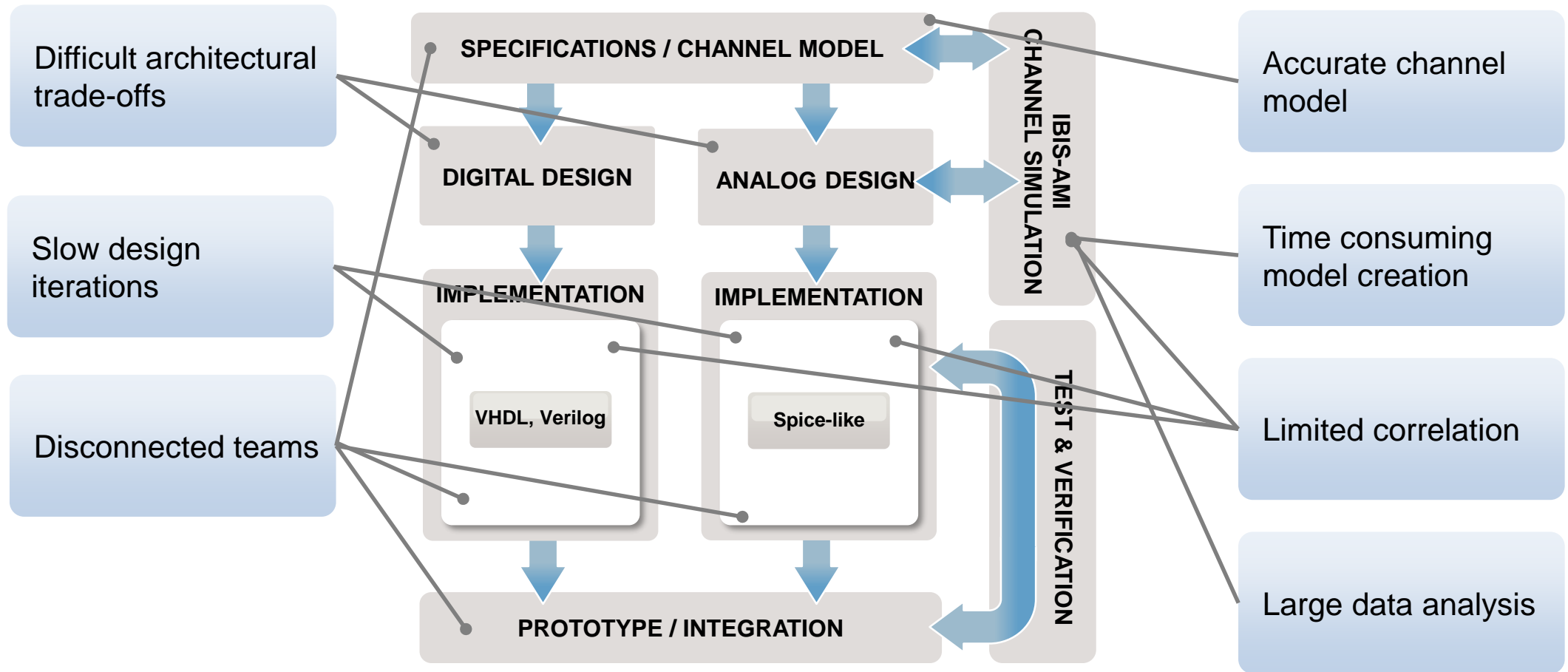
4



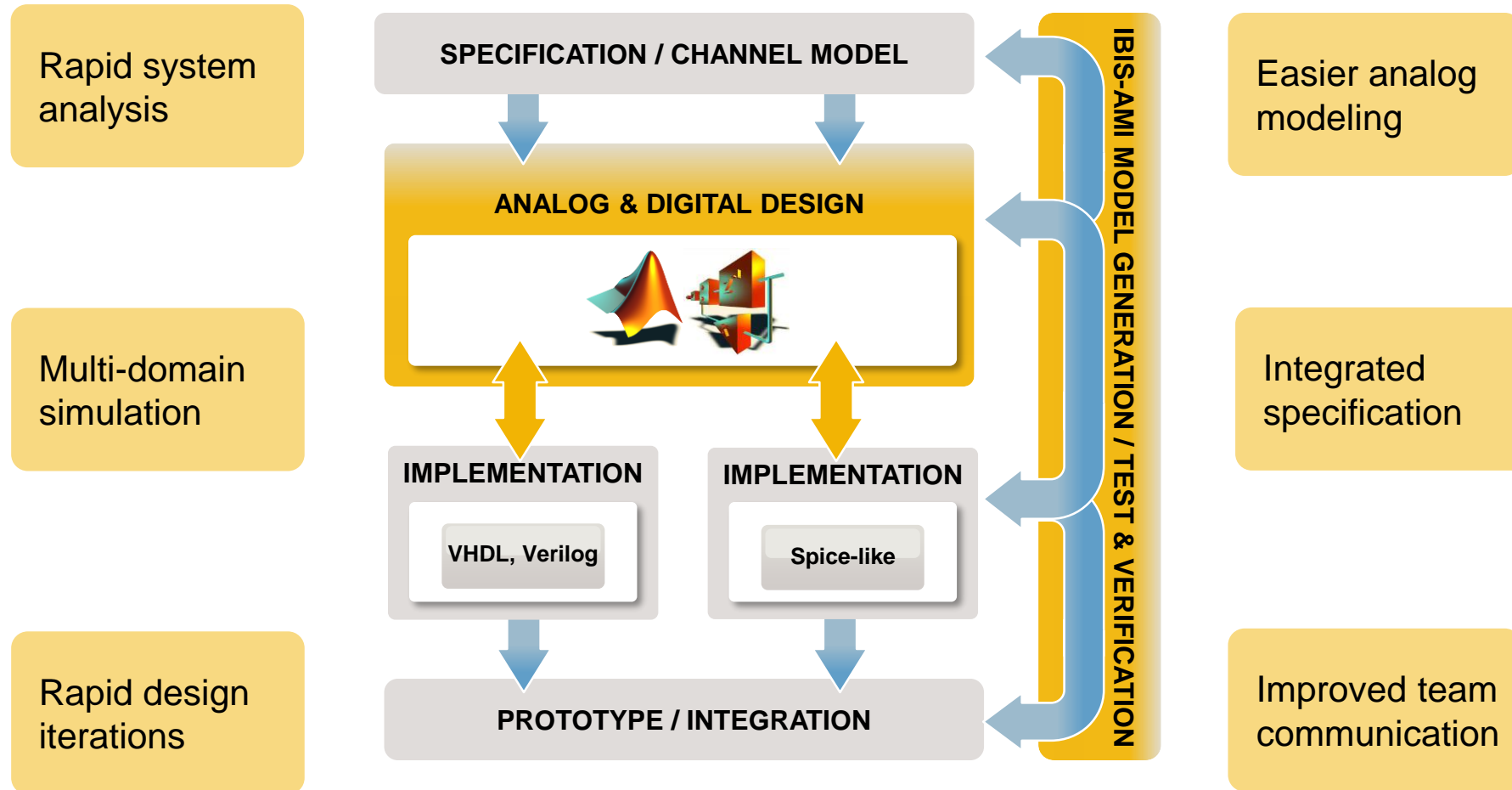
A Typical SerDes System: TX, RX, and Channel



SerDes Design and Verification Challenges

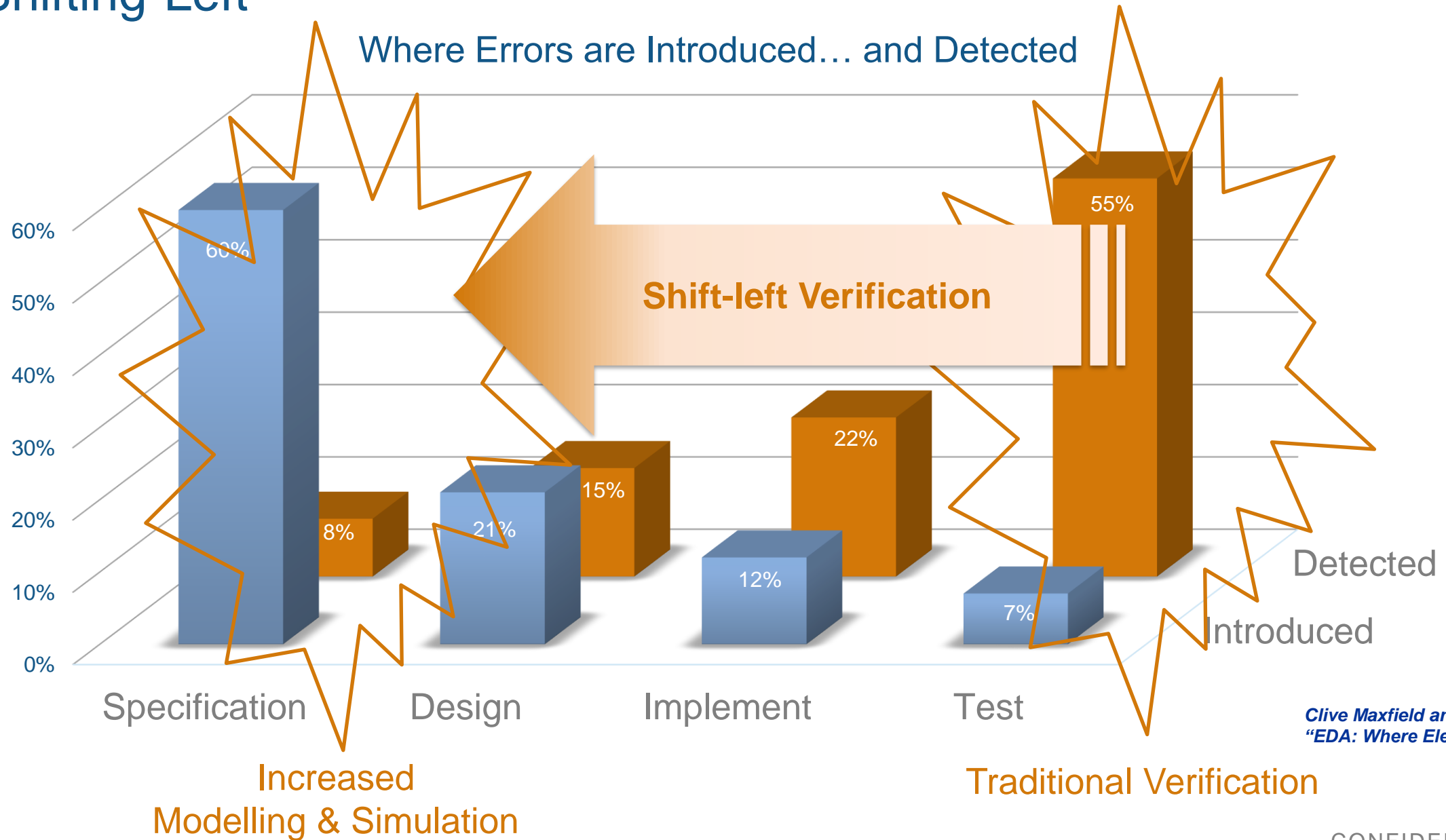


System-Level Design and Analysis Leads to Continuous Verification



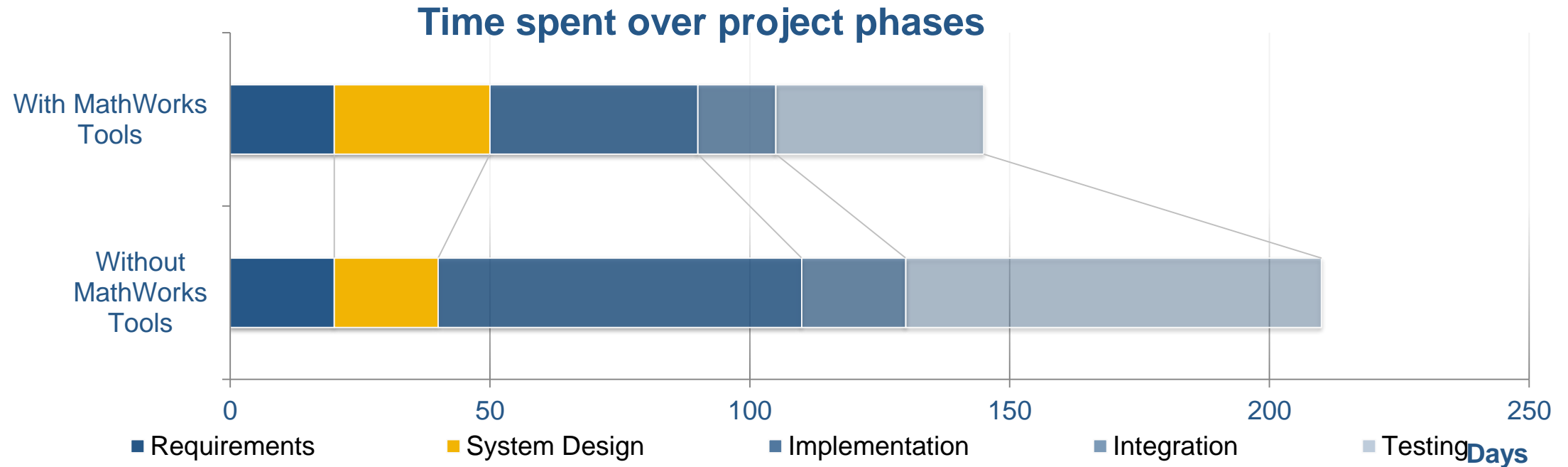
Shifting-Left

Where Errors are Introduced... and Detected



Clive Maxfield and Kuhoo Goyal
"EDA: Where Electronics Begins"

Save 30% of Overall Development Time (and improve quality, reduce re-spins, etc.)



EE Times - Top-down verification guides mixed-signal designs

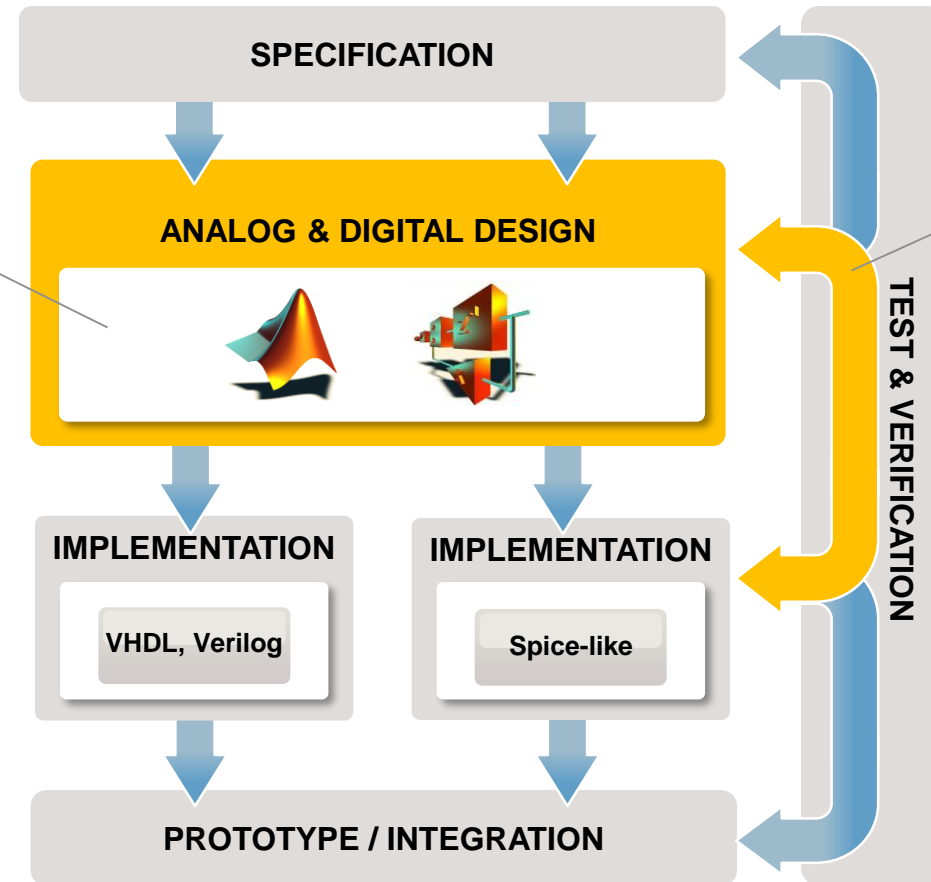
[K. Kundert and H. Chang, Partners, Designer's Guide Consulting](#)

*“In order to address these challenges, many design teams are either looking to, or else have already implemented, a **top-down design methodology**. In a top-down approach, the architecture of the chip is defined as a block diagram and simulated and optimized using a system simulator such as **MATLAB or Simulink**. From the high-level simulation, requirements for the individual circuit blocks are derived.”*

What's New

R2019a

SerDes Toolbox

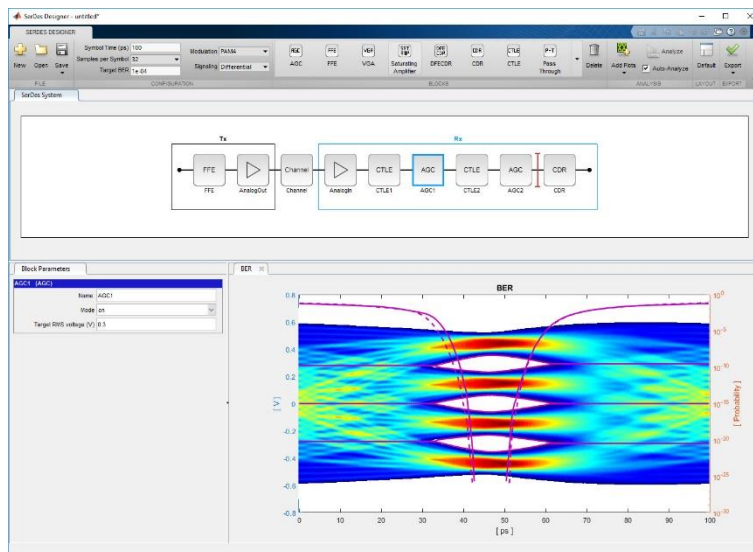


Integration with IC design tools and channel simulators

R2019a SerDes Toolbox

Design SerDes systems and generate IBIS-AMI models for high-speed digital interconnects

- Design and analyze transmitters and receivers with the SerDes Designer app
- Develop equalization algorithms with MATLAB System objects and Simulink blocks
 - FFE, DFE, AGC, CDR, CTLE, etc...
- Perform SerDes statistical analysis and time-domain simulation
- Generate dual IBIS-AMI models for 3rd party channel simulators
- Use reference designs for high-speed links such as Ethernet CEI-56G, DDR5, PCI-Gen4, USB3.1

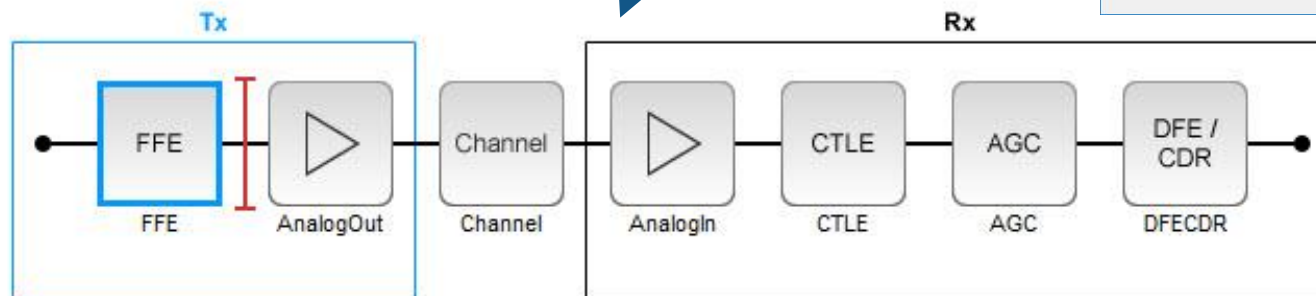
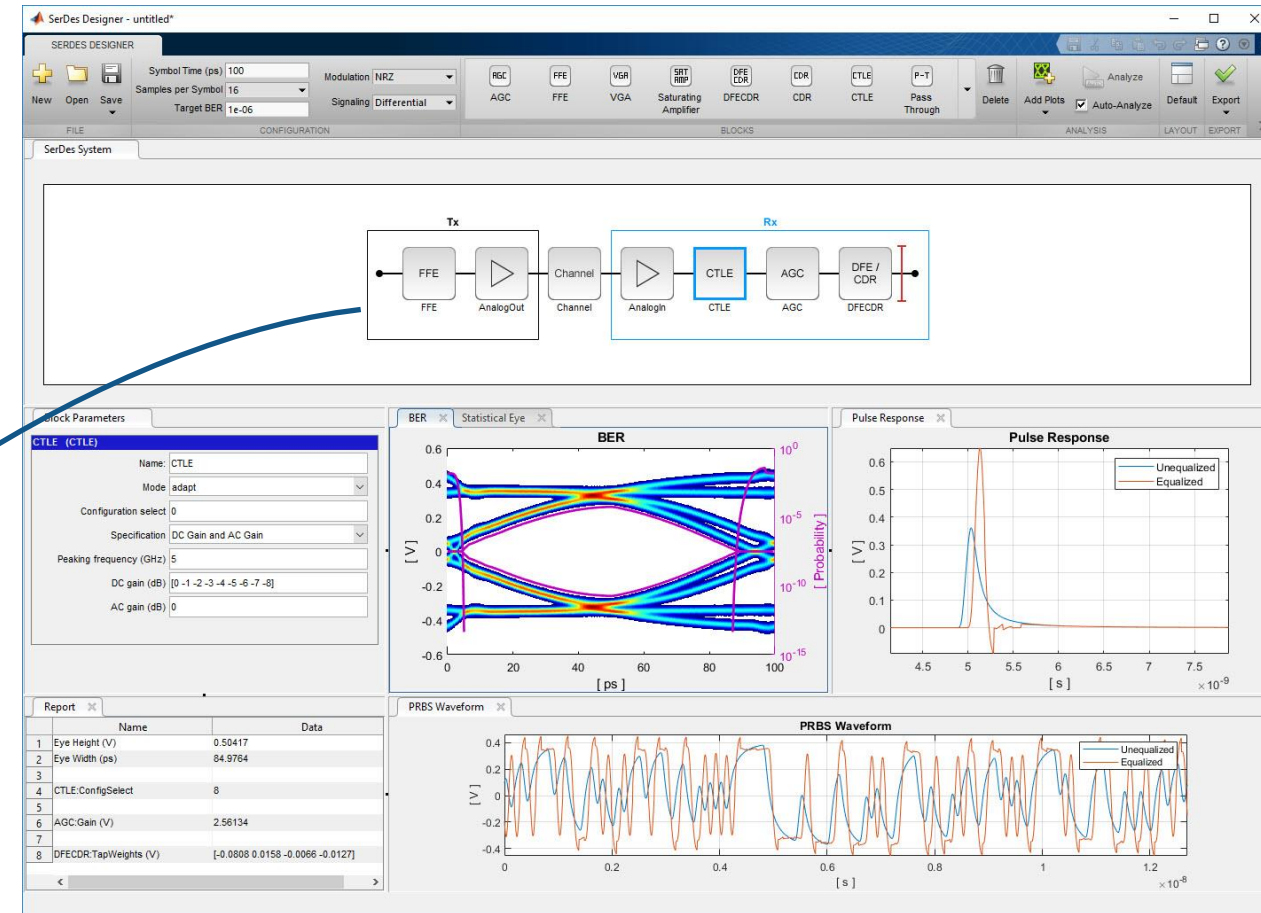


This composite image illustrates the configuration of a stimulus block in the SerDes Designer app. On the left, a block diagram shows a 'Stimulus' block connected to a 'Channel' block, which is then connected to an 'Eye Diagram' block. The 'Stimulus' block is highlighted with a yellow box. In the center, the 'Block Parameters: Stimulus' dialog box is open, showing the 'Modulation Select' dropdown menu with 'NRZ' selected. The 'PRBS Select' is set to 7. On the right, a code snippet shows the configuration for the stimulus block in a MATLAB script:

```
1 (Rx
2 (Reserved_Parameters
3 (AMI_Version (Usage Info) (Type String) (Default "6.0") (Description "AMI_Version"))
4 (Init_Returns_Impulse (Usage Info) (Type Boolean) (Default False) (Description "Init_Returns_Impulse"))
5 (GetWave_Exists (Usage Info) (Type Boolean) (Default True) (Description "GetWave_Exists"))
6 (Max_Init_Aggressors (Usage Info) (Type Integer) (Default 32) (Description "Max_Init_Aggressors"))
7 (Ignore_Bits (Usage Info) (Type Integer) (Default 0) (Description "Ignore_Bits"))
8 )
9 (Model_Specific
10 (CTLEParameter
11 (Mode (Usage In) (Type Float) (Format Value 1.0) (Description "CTLE Mode: 0=off, 1=fix"))
12 (ConfigSelect (Usage In) (Type Float) (Format Range 1.0 1.0 1.0) (Description "CTLE ConfigSelect"))
13 )
14 (AGCParameter
15 (Mode (Usage In) (Type Float) (Format Value 1.0) (Description "AGC Mode: 0=off, 1=on"))
16 (TargetRMSVoltage (Usage In) (Type Float) (Format Range 0.1 0.001 10.0) (Description "AGC TargetRMSVoltage"))
17 )
18 (Modulation (Usage In) (Type Float) (Format Value 2.0))
19 (SatAmpParameter
20 (Mode (Usage In) (Type Float) (Format Value 0.0) (Description "Saturation amplifier mode"))
```

SerDes Designer app: No Need to be a SerDes Expert

- Design and analyze SerDes systems including transmitters and receivers with arbitrary configuration
- Use parameterized building blocks
- Perform statistical analysis: eye diagram, BER, bathtub, pulse response....



SerDes Design: Where to Start?

Add SerDes components

- Export to:
- MATLAB
 - Simulink
 - IBIS-AMI

- Modulation
- Sample rate
- Signaling

The screenshot shows the SerDes Designer software interface. At the top, the configuration panel includes fields for Symbol Time (ps) set to 100, Samples per Symbol set to 16, and Target BER set to 1e-06. Below this is a toolbar with various SerDes components like AGC, FFE, VGR, SRT AMP, DFE/CDR, CDR, CTLE, and P-T. A central block diagram shows a Tx path (FFE, AnalogOut, Channel) and an Rx path (AnalogIn, CTLE, AGC, DFE/CDR). The bottom section contains several analysis plots: a BER plot showing eye diagrams, a Pulse Response plot comparing Unequalized and Equalized signals, and a PRBS Waveform plot. A 'Block Parameters' window for the CTLE block is open, showing settings like Mode (adapt), Specification (DC Gain and AC Gain), and Peaking frequency (5 GHz).

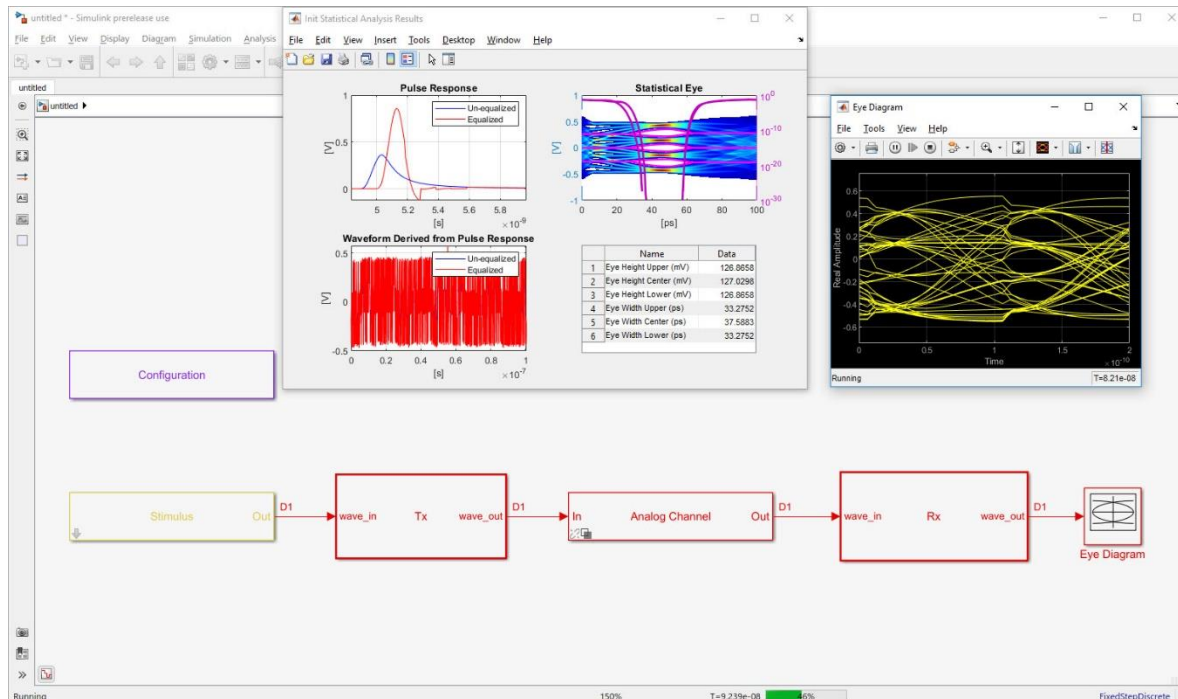
Plot analysis results

High-speed link

Component specifications

SerDes Top Down Design

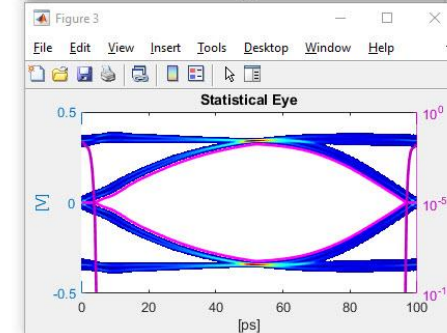
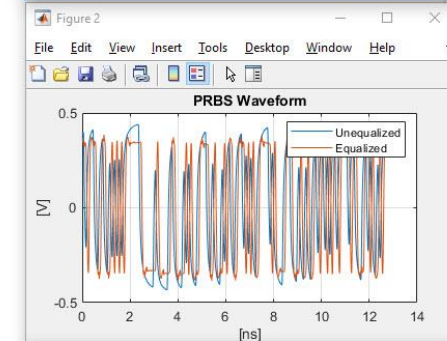
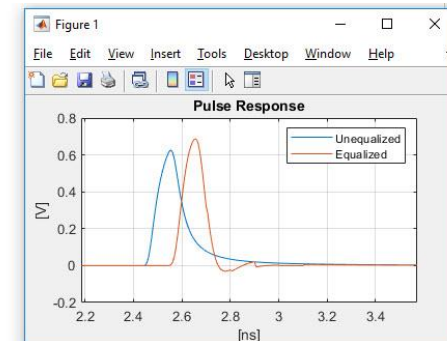
- Create a MATLAB script for automation and design space exploration
- Export to Simulink models for time-domain simulation
- Create dual IBIS-AMI models



```

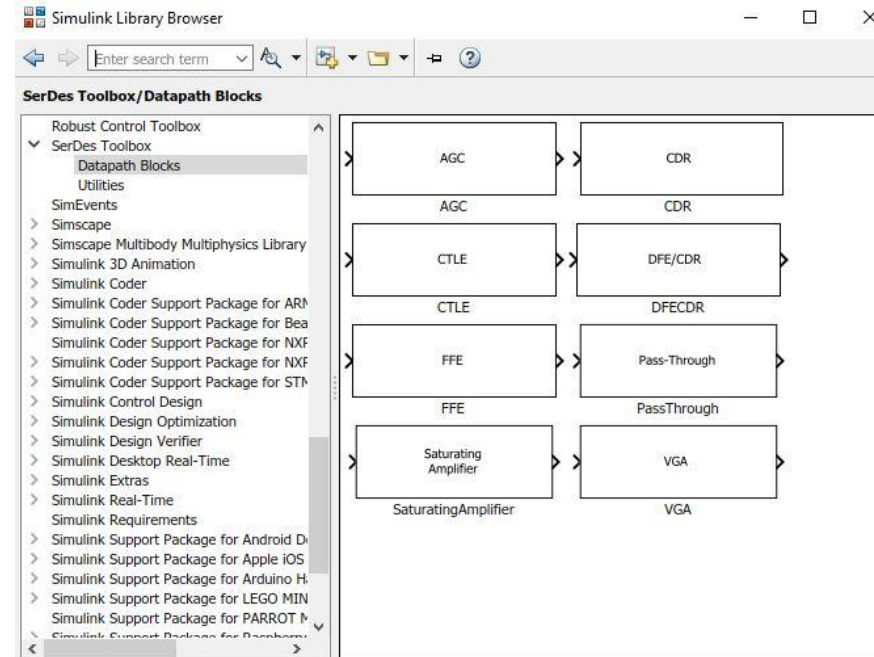
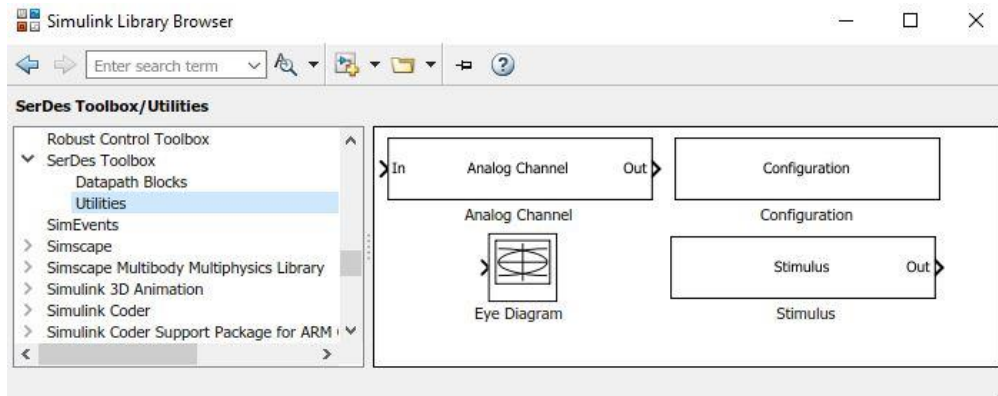
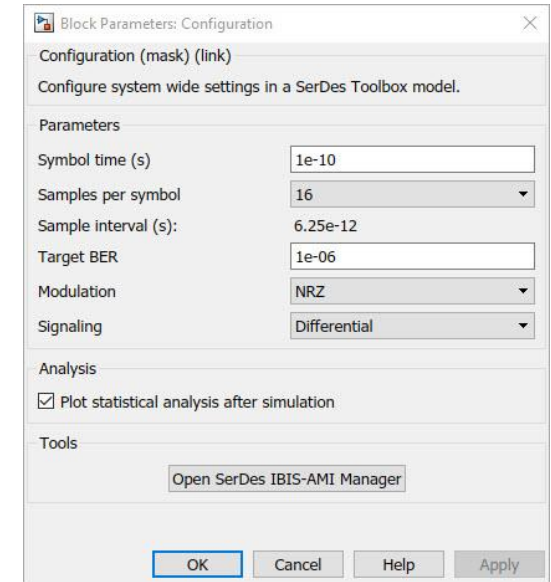
1 %-----
2 % MATLAB script to build SerDes System
3 %-----
4
5
6 % Build cell array of Tx blocks:
7 txBlocks(1) = serdes.FFE;
8 txBlocks(1).BlockName = 'FFE';
9 txBlocks(1).Mode = 1;
10 txBlocks(1).TapWeights = [0 1 0 0 0];
11 txBlocks(1).Normalize = true;
12
13 % Build cell array of Rx blocks:
14 rxBlocks(1) = serdes.CTLE;
15 rxBlocks(1).BlockName = 'CTLE';
16 rxBlocks(1).Mode = 2;
17 rxBlocks(1).ConfigSelect = 0;
18 rxBlocks(1).Specification = 'DC Gain and Peaking Gain';
19 rxBlocks(1).PeakingFrequency = 5000000000;
20 rxBlocks(1).DCGain = [0 -1 -2 -3 -4 -5 -6 -7 -8];
21 rxBlocks(1).PeakingGain = [0 1 2 3 4 5 6 7 8];
22
23 rxBlocks(2) = serdes.AGC;
24 rxBlocks(2).BlockName = 'AGC';
25 rxBlocks(2).Mode = 1;
26 rxBlocks(2).TargetRMSVoltage = 0.3;
27
28 rxBlocks(3) = serdes.DFECDR;
29 rxBlocks(3).BlockName = 'DFECDR';
30 rxBlocks(3).Mode = 2;
31 rxBlocks(3).TapWeights = [0 0 0 0];
32 rxBlocks(3).MinimumTap = -1;
33 rxBlocks(3).MaximumTap = 1;
34
35 % Build txModel:
36 txAnalogModel = AnalogModel( ...
37     'R',50, ...
38     'C',1.000000e-13);
39 tx = Transmitter( ...
40     'Blocks',txBlocks, ...
41     'AnalogModel',txAnalogModel, ...
42     'RiseTime',1.000000e-11, ...
43     'VoltageSwingIdeal',1, ...
44     'Name','TX');
45
46 % Build rxModel:
47 rxAnalogModel = AnalogModel( ...
48     'R',50, ...
49     'C',2.000000e-13);
50 rx = Receiver( ...
51     'Blocks',rxBlocks, ...
52     'AnalogModel',rxAnalogModel, ...
53     'Name','RX');
54
55 % Build ChannelData:
56 channel = ChannelData( ...
57     'ChannelLossB',8, ...
58     'ChannelLossFreq',5000000000, ...
59     'ChannelDifferentialImpedance',100);
60
61 % Build SerDes System:
62 SymbolTime = 1e-10;
63 SamplesPerSymbol = 16;
64 ModulationLevels = 2;
65 BERtarget = 1e-06;
66

```



SerDes Toolbox: Simulink Models

- Develop adaptive equalizers using white-box models such as DFE, CTLE, AGC, and CDR
- Use parametrized blocks and algorithms for single-ended and differential signals
- Generate PRBS and custom stimulus patterns supporting PAM4 and NRZ modulation



SerDes Simulation and Architecture Exploration

Configuration



Global Parameters

The screenshot shows the 'Global Parameters' window in the SerDes IBIS-AMI Manager. The 'Node Details' for 'PAM4_UpperThreshold' are visible, including its description, type (Float), usage (Out), format (Value), and current value (0.333).

Channel modeling

The 'Block Parameters: Analog Channel' dialog box shows the configuration for the Analog Channel block. It includes fields for Channel Model (Impulse response), Impulse response (zeros(1,63),1/SampleInterval,zeros(1,192)), and Analog Model parameters (Tx R, Rx R, Tx C, Rx C, Rise time, Voltage).

White-box (customizable) models

```

%Note that step or time domain adaptation of the CTLE must be
%done in an exterior block.

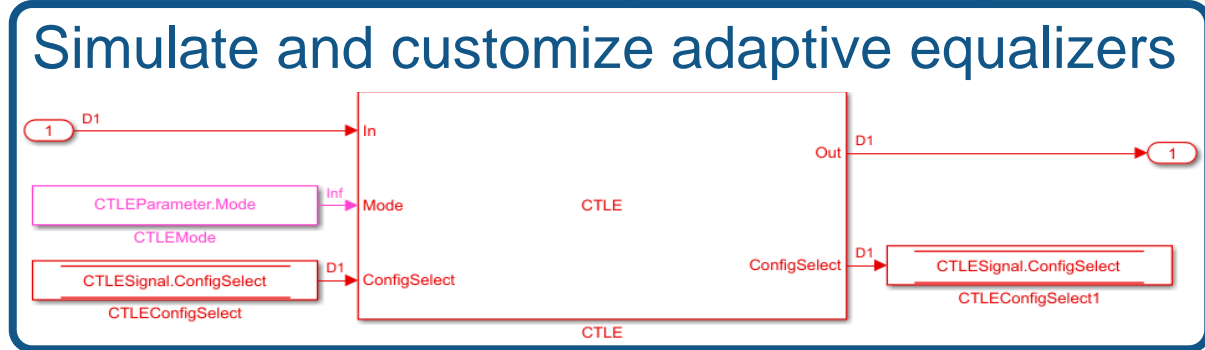
fixed(obj)
= obj.ConfigSelect;|

privConfigInitialFlag
obj.privConfigInitial = obj.ConfigSelect;
obj.privConfigInitialFlag = false;

obj.privConfigInitial = obj.ConfigSelect;

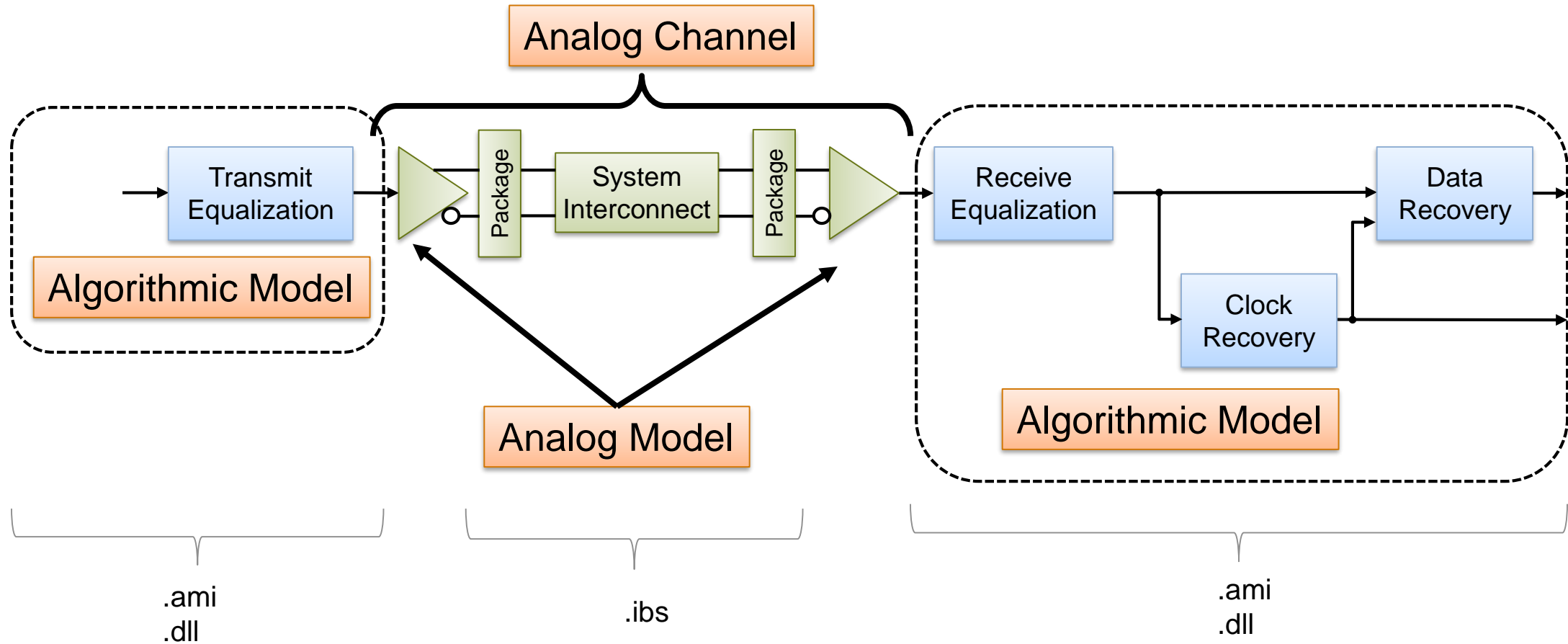
= obj.privConfigInitial;

obj.FilterCoefficients.np(Config+1)+1;
obj.FilterCoefficients.nz(Config+1)+1;
    
```

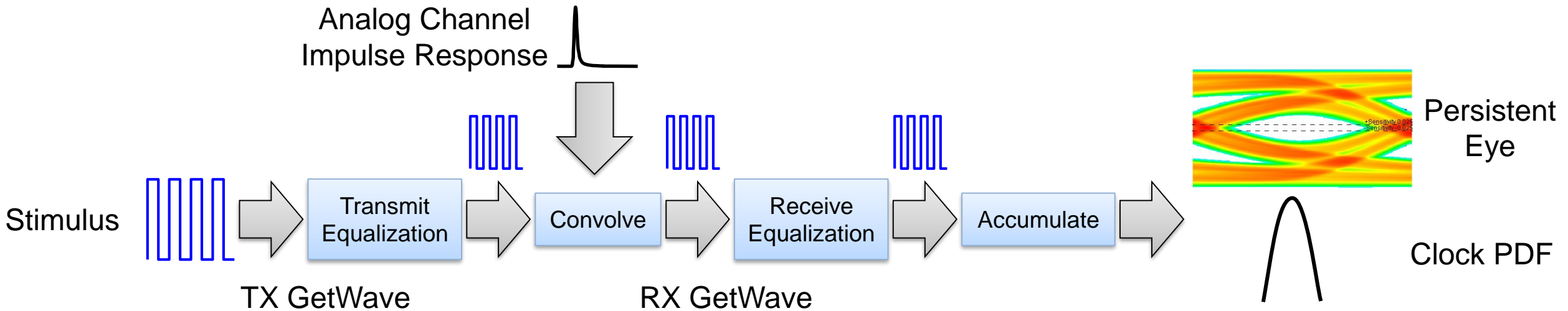
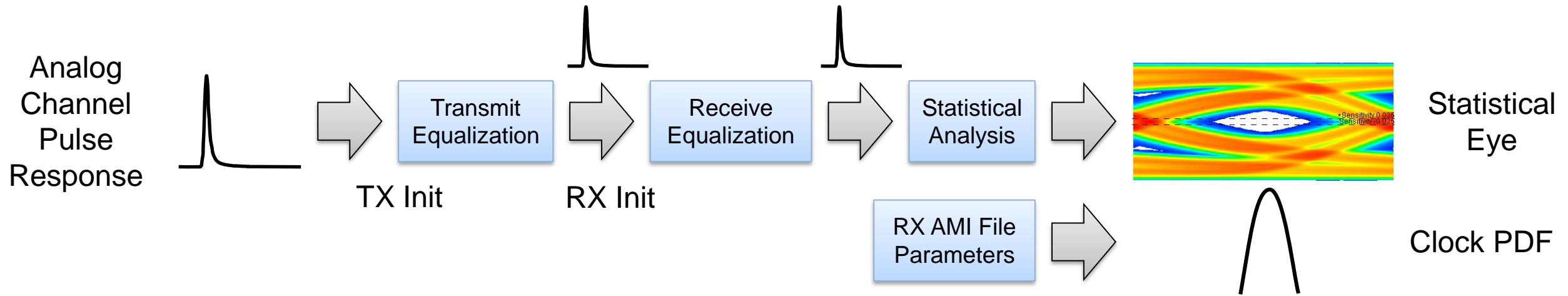


Automatic Generation of Standard Compliant IBIS-AMI Models

IBIS-AMI Terminology

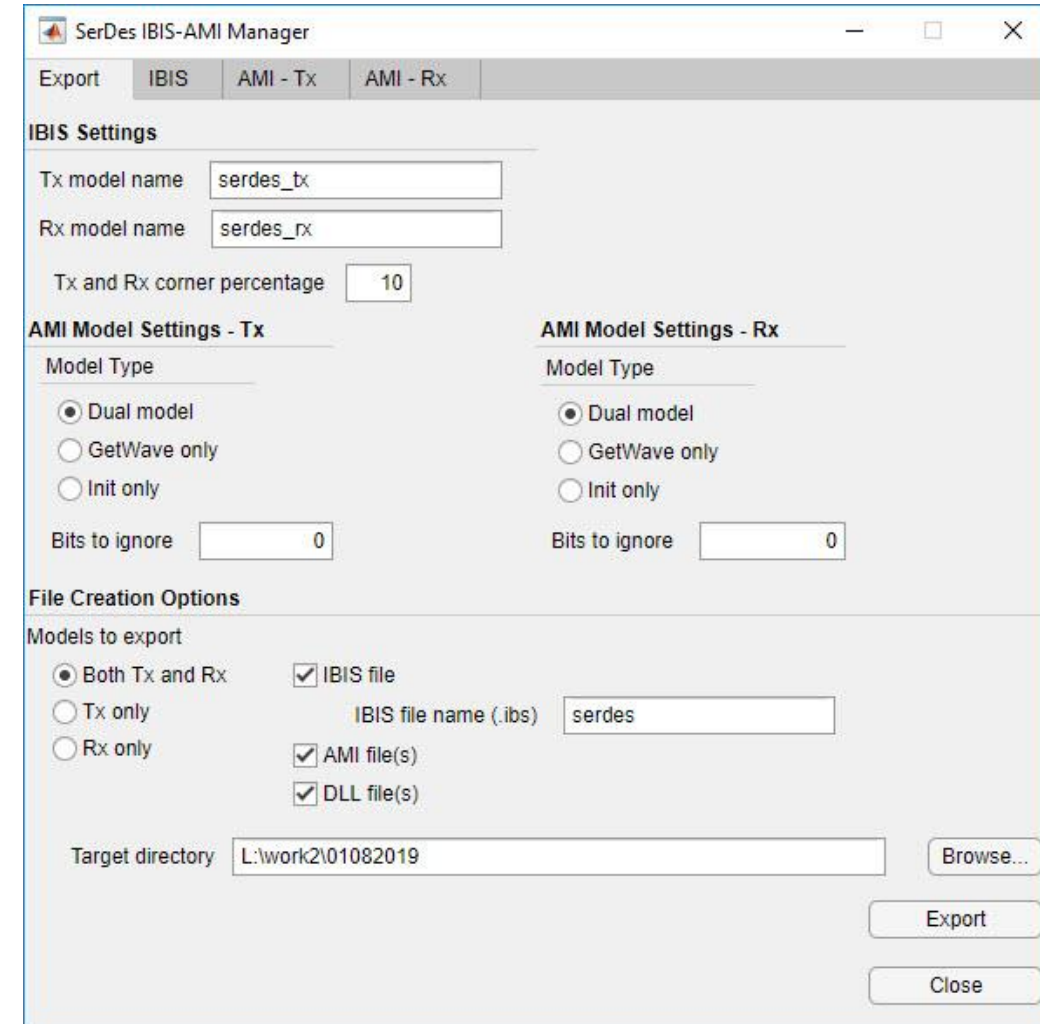
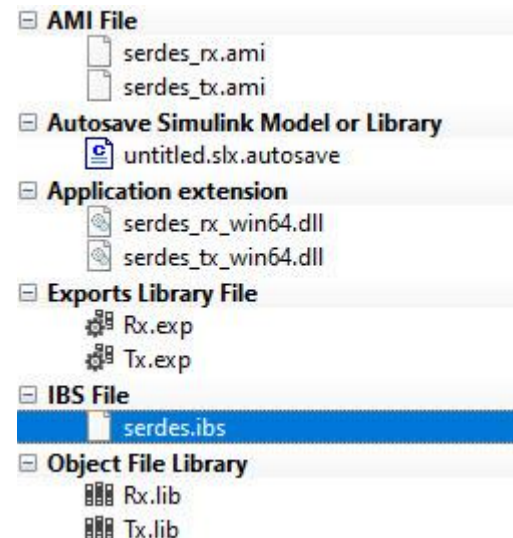


Statistical vs. Time Domain



SerDes Toolbox: IBIS-AMI Dual Model Generation

- Generate standard-compliant Init and GetWave IBIS-AMI models
- Generate associated analog IBIS model
- Customize the model interface by managing the IBIS-AMI-parameters



SerDes Verification Using Channel Simulators

Channel Simulation Using IBIS-AMI Models

- Integrate standard-compliant IBIS-AMI models in 3rd party channel simulators
 - Correlation & regression testing
 - Identification of corner cases over large families of channel models and configurations

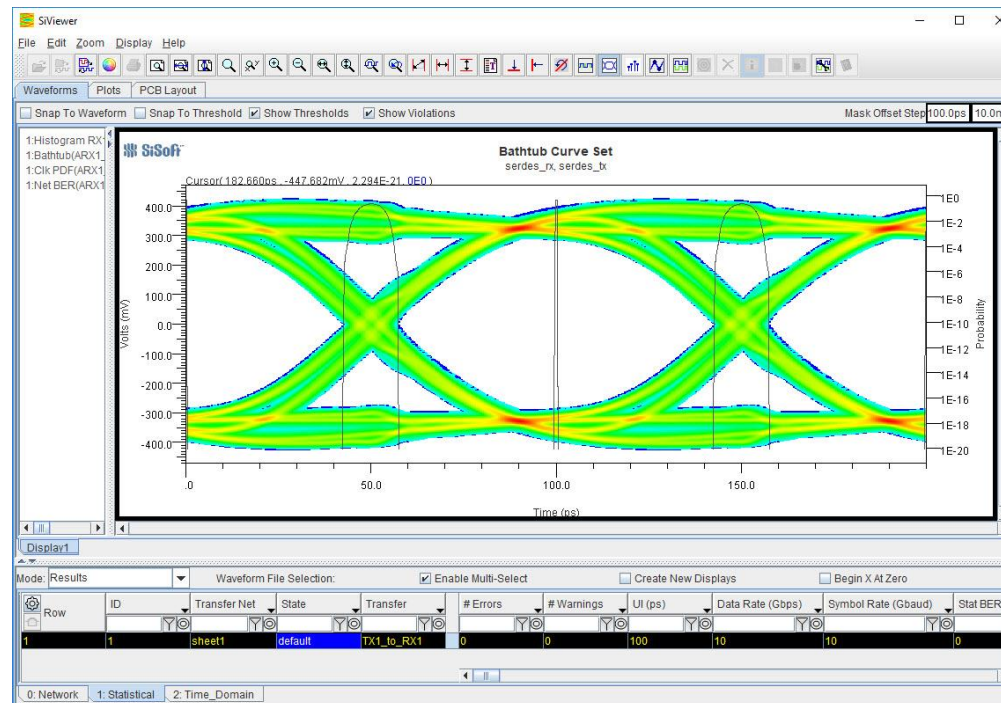
The screenshot displays the Quantum Channel Designer 300 interface. The main workspace shows a schematic diagram of a channel simulation. On the left, a transmitter model is labeled "TX1 serdes Tx serdes_tx 200.0ps - 200ps None". It is connected to a channel consisting of three differential strip lines, labeled "W1", "W2", and "W3", with parameters like "\$W1:Length", "\$W2:Length", and "\$W3:Length". On the right, a receiver model is labeled "RX1 serdes Rx serdes_rx". Below the schematic, the state is set to "default" and the topology to "sheet1".

The "Solution Space" table at the bottom lists various variables and their values for different sheets:

Transfer Net	Variable	Type	Format	Variation Group	Value 1	Value 2
sheet1	Ech	Corner	List	Corners	TE (Typ)	
sheet1	Process	Corner	List	Corners	TT (Typ)	
sheet1	RX1.CTLE.Mode	Integer	AM List	<none>	adapt	
sheet1	RX1.CTLE.ConfigSelect	Integer	AM Range	<none>	0	
sheet1	RX1.AGC.Mode	Integer	AM List	<none>	on	
sheet1	RX1.AGC.TargetRMSVoltage	Float	AM Range	<none>	0.3	
sheet1	RX1.DFECOR.ReferenceOffset	Float	AM Range	<none>	0	
sheet1	RX1.DFECOR.PhaseOffset	UI	AM List	<none>	0	
sheet1	RX1.DFECOR.Mode	Integer	AM List	<none>	adapt	
sheet1	RX1.DFECOR.TapWeights.1	Tap	AM Range	RX1.Tap	0	
sheet1	RX1.DFECOR.TapWeights.2	Tap	AM Range	RX1.Tap	0	
sheet1	RX1.DFECOR.TapWeights.3	Tap	AM Range	RX1.Tap	0	
sheet1	RX1.DFECOR.TapWeights.4	Tap	AM Range	RX1.Tap	0	
sheet1	TX1.OptmEye	String	AM List	<none>	OE	
sheet1	TX1.FFE.Mode	Integer	AM List	<none>	fixed	
sheet1	TX1.FFE.TapWeights.-1	Tap	AM Range	TX1.Tap	0	
sheet1	TX1.FFE.TapWeights.0	Tap	AM Range	TX1.Tap	1	
sheet1	TX1.FFE.TapWeights.1	Tap	AM Range	TX1.Tap	0	
sheet1	TX1.FFE.TapWeights.2	Tap	AM Range	TX1.Tap	0	

Integration with QCD/QSI (SiSoft Link)

- Bidirectional link between SerDes Toolbox and SiSoft QCD/QSI
- Automatically create a QCD/QSI project from SerDes Toolbox
- Back-annotate the channel model, stimuli, and AMI parameter settings into SerDes Toolbox
- Rapidly iterate between system design and channel simulation



Use Simulink and SerDes Toolbox

- Algorithmic design, analysis, and system-level simulation of SerDes systems with many trusted functions
- Integrate with 3rd party channel simulators for SerDes verification
 - Generate standard-compliant IBIS-AMI models
- Link with IC design tools to model implementation impairments and reuse testbenches
 - Co-simulation, HDL/SV code generation, and data post-processing

Thank You!
Q&A